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| 09/975,257 | 10/12/2001 | Sundar Narayanan | 8229-013-27 | 8852 |

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| EXAMINER | |
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| DOTY, HEATHER ANNE | |

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| 2813 | |

DATE MAILED: 04/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/975,257 | Applicant(s) NARAYANAN ET AL. | |
|---|---|---|---|
| | Examiner Heather A. Doty | Art Unit 2813 | |

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *31 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3,5-19 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-19 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 5-12, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasushi (JP 2000-311928, published 11/7/2000) in view of Bensahel et al. (U.S. 6,372,581).

Regarding claim 1, Yasushi teaches a method of determining the nitrogen content of a nitrided gate oxide layer on a semiconductor substrate comprising:

nitriding a gate oxide layer (**2**) on a semiconductor substrate (**1**) to form the nitrided gate oxide layer (**3**) on the substrate;

oxidizing the nitrided gate oxide layer on the substrate, wherein the step of oxidizing the nitrided gate oxide layer distances the nitrided gate oxide layer away from the semiconductor substrate (Yasushi does not expressly teach this effect, but since Yasushi teaches reoxidizing the nitrided gate manner by heating the sample in an oxygen atmosphere—page 2, lines 6-8 of the translation—the same method disclosed by Applicant, it is inherent that the step of oxidizing the nitrided gate oxide layer taught by Yasushi will also distance the nitrided gate oxide layer away from the semiconductor substrate);

measuring the thickness (L2) of the oxidized nitrided gate oxide layer (**4**);

optionally calculating the change in thickness of the oxidized nitrided gate oxide layer; and

determining if the measured thickness or calculated change in thickness of the oxidized nitrided gate oxide layer exceeds a target thickness (40 Å—Fig. 1 and 2, abstract, and pg. 2 of translation).

Yasushi does not teach using nitric oxide (NO) to nitride the gate oxide layer.

Bensahel et al. teaches that it is known in the art to substitute NO for $N_2O$ to nitride a gate oxide layer because $N_20$ is ineffective for nitriding thin oxide layers (column 1, lines 35-40).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Yasushi and substitute NO for $N_2O$ to nitride the gate oxide layer because it is known in the art to use either NO or $N_2O$ for this purpose, and furthermore, $N_2O$ is ineffective for nitriding thin oxide layers, as expressly taught by Bensahel et al.

Regarding claim 3, Yasushi and Bensahel et al. together teach the method of claim 1. Yasushi further teaches correlating the measured thickness or change in thickness of the oxidized nitrided gate oxide layer with the nitrogen content of the gate oxide layer (abstract and pg. 2 of translation).

Regarding claim 5, Yasushi and Bensahel et al. together teach the method of claim 1. Yasushi further teaches forming the gate oxide layer on the substrate prior to the nitriding step (Fig. 1, pg. 2).

Regarding claim 6, Yasushi and Bensahel et al. together teach the method of claim 3. Yasushi further teaches that the correlating step comprises measuring the oxidized nitrided gate oxide for a plurality of samples, each having a known nitrogen content; optionally calculating the change in thickness after oxidizing the nitrided gate oxide layer for each sample; and performing a least-squares regression analysis to generate a calibration curve for nitrogen content of the nitrided gate oxide as a function of oxidized nitrided gate oxide thickness or change in oxidized nitrided gate oxide thickness (see Fig. 2 and pg. 2).

Regarding claim 7, Yasushi and Bensahel et al. together teach the method of claim 1. Yasushi further teaches that the step of determining the change in thickness of the oxidized nitrided gate oxide layer comprises determining an initial gate oxide thickness by measuring the thickness of the gate oxide layer prior to the oxidation step (L1) and calculating the difference between the measured oxidized nitrided gate oxide layer thickness and the initial gate oxide thickness (pg. 2—[(L2-L1)/T]).

Regarding claim 9, Yasushi and Bensahel et al. together teach the method of claim 7. Yasushi further teaches measuring the initial gate oxide thickness after the nitridation step (L1—pg. 2).

Regarding claim 10, Yasushi teaches a method of determining the nitrogen content of a nitrided gate oxide layer on a semiconductor substrate comprising:

nitriding a gate oxide layer (**2**) on a semiconductor substrate (**1**) to form the nitrided gate oxide layer (**3**) on the substrate;

oxidizing the nitrided gate oxide layer on the substrate wherein the step of oxidizing the nitrided gate oxide layer distances the nitrided gate oxide layer away from the semiconductor substrate (Yasushi does not expressly teach this effect, but since Yasushi teaches reoxidizing the nitrided gate manner by heating the sample in an oxygen atmosphere—page 2, lines 6-8 of the translation—the same method disclosed by Applicant, it is inherent that the step of oxidizing the nitrided gate oxide layer taught by Yasushi will also distance the nitrided gate oxide layer away from the semiconductor substrate);

measuring the thickness (L2) of the oxidized nitrided gate oxide layer (**4**);

calculating the change in thickness of the oxidized nitrided gate oxide layer; and

determining if the measured thickness or calculated change in thickness of the oxidized nitrided gate oxide layer exceeds a target thickness value (40 Å), wherein calculating the change in thickness of the oxidized nitrided gate oxide layer comprises determining an initial gate oxide thickness (measuring L1) prior to the oxidation step and calculating the difference between the measured oxidized nitrided gate oxide layer thickness and the initial gate oxide thickness ([(L2-L1)/T]; Fig. 1 and 2, abstract, and pg. 2 of translation).

Yasushi does not teach using nitric oxide (NO) to nitride the gate oxide layer.

Bensahel et al. teaches that it is known in the art to substitute NO for $N_2O$ to nitride a gate oxide layer because $N_20$ is ineffective for nitriding thin oxide layers (column 1, lines 35-40).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Yasushi and substitute NO for $N_2O$ to nitride the gate oxide layer because it is known in the art to use either NO or $N_2O$ for this purpose, and furthermore, $N_2O$ is ineffective for nitriding thin oxide layers, as expressly taught by Bensahel et al.

Regarding claim 12, Yasushi and Bensahel et al. together teach the method of claim 1. Yasushi further teaches measuring the concentration of nitrogen in a gate oxide layer (abstract and pg. 2). Although Yasushi does not explicitly teach forming the gate electrode layer, the Examiner deems this step inherent to the disclosure of Yasushi, since the scope of Yasushi's teaching entails a method for measuring the nitrogen concentration specifically in a gate oxide film (see MPEP 2112).

Regarding claim 8, Yasushi and Bensahel et al. together teach the method of claim 7, but do not teach measuring the initial gate oxide thickness before the nitridation step.

However, the instant specification contains no disclosure of either the critical nature of the claimed process (measuring the gate oxide thickness before the nitridation step), or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the Applicant must show that the chosen limitations are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990).

In light of Applicant's failure to establish criticality, the limitation of measuring the gate oxide thickness before the nitridation step is deemed equivalent to the limitation of measuring the gate oxide thickness after the nitridation step.

Regarding claim 11, Yasushi and Bensahel et al. together teach the method of claim 10, but do not teach that the initial gate oxide thickness is estimated from previously collected gate oxide thickness data.

However, the instant specification contains no disclosure of either the critical nature of the claimed process (estimating the gate oxide thickness from previously collected gate oxide thickness data), or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the Applicant must show that the chosen limitations are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990).

In light of Applicant's failure to establish criticality, the limitation of estimating the gate oxide thickness from previously collected gate oxide thickness data is deemed equivalent to estimating the gate oxide thickness via measurement.

Regarding claim 17, Yasushi and Bensahel et al. together teach the method of claim 1. Yasushi further teaches that the oxidizing step is performed in the same tool as the nitridation step (pg. 2).

Regarding claim 18, Yasushi and Bensahel et al. together teach the method of claim 1, but do not teach that the nitridation step is performed in a first tool and the substrate is transferred to a different tool for the oxidizing step.

However, the Examiner deems performing the oxidation and nitridation steps in the same chamber as equivalent to performing oxidation and nitridation in different tools, since the end results are the same.

Finally, the specification contains no disclosure of either the critical nature of the claimed process or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the Applicant must show that the chosen limitations are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990).

Claim 2 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasushi (JP 2000-311928, published 11/7/2000) in view of Bensahel et al. (U.S. 6,372,581), as applied to claims 1 and 12 above, and further in view of Wolf et al. (*Silicon Processing for the VLSI Era*, vol. 1-3).

Regarding claim 2, Yasushi and Bensahel et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above), but do not teach that the oxidizing step comprises rapid thermal oxidation of the nitrided gate oxide layer in a rapid thermal processing (RTP) chamber.

However, Wolf et al. teaches that RTP is emerging as the tool of choice for growth of ultra-thin gate oxides and oxynitrides (vol. 1, pg. 310). Furthermore, Wolf et al. teaches that RTP allows for reduced thermal budget and a short processing times at high temperatures (vol. 1, pg. 309).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Yasushi and Bensahel et al.

together, and also taught by claim 1, and further perform the oxidizing step by rapid thermal oxidation in an RTP chamber, which allows for reduced thermal budget, as expressly taught by Wolf et al.

Regarding claim 13, Yasushi and Bensahel et al. together teach the method of claim 12 (note 35 U.S.C. 103(a) rejection above), but they do not teach a step of implanting boron atoms in the gate electrode layer.

However, Wolf et al. teaches that it is known in the art to implant boron into a polysilicon gate electrode to make a p+ gate electrode, particularly with thin-oxide devices, to decrease punchthrough problems (vol. 3, pgs. 311-312).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Yasushi and Bensahel et al. together, and also taught by claim 12, and further implant boron into the gate electrode to decrease punchthrough problems, as expressly taught by Wolf et al.

Regarding claim 14, Yasushi and Bensahel et al. together teach the method of claim 12, but do not teach that the predetermined value corresponds to a nitrogen content sufficient to prevent boron atoms from diffusing through the gate oxide layer and into the semiconductor substrate.

However, Wolf et al. teaches that a gate oxide subjected to nitridation with provide a barrier to boron migration (vol. 3, pgs. 313 and 649).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Yasushi and Bensahel et al. together, and also taught by claim 12, and incorporate a gate oxide subjected to

nitridation that will provide a barrier to boron migration, as taught by Wolf et al. to be well known in the art.

Regarding claims 15 and 16, Yasushi and Bensahel et al. together teach the method of claim 1, but do not teach that the oxidation step is conducted at a temperature of 900 to 1025 °C, or for 10 minutes or less.

However, Wolf et al. teaches reoxidation of a nitrided gate oxide layer at a temperature of 950 to 1150 °C for about 60 seconds (vol. 3, pgs. 653). Furthermore, Wolf et al. teaches that these are common process conditions for the reoxidation of a nitrided oxide layer.

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Yasushi and Bensahel et al. together, and incorporate the reoxidation of a nitrided gate oxide layer at a temperature of 950 to 1150 °C for about 60 seconds, as taught by Wolf et al. to be process conditions commonly employed in the art to form a reoxidized nitrided gate oxide layer.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li (U.S. 5,862,054) in view of Yasushi (JP 2000-311928, published 11/7/2000) and Bensahel et al. (U.S. 6,372,581).

Regarding claim 19, Li teaches collecting process parameter data for each batch (**30**); storing parameter data in a database (**32**); computing an average value for each stored parameter (**32**); storing the average values in a historical data file on a computer (**33**); determining process control limits from the stored historical data file (**34**); and monitoring the process parameters and comparing these values to control limits (Fig. 3;

column 4, lines 1-20). Li also inherently teaches that any of the above steps can be repeated to obtain necessary data for statistical process control.

Li does not teach for each substrate in a batch of semiconductor substrates, nitriding a gate oxide layer on the semiconductor substrate using nitric oxide gas to form the nitrided gate oxide layer on the substrate, and oxidizing the nitrided gate oxide layer on the substrate to form an oxidized nitrided gate oxide layer, wherein the step of oxidizing the nitrided gate oxide layer distances the nitrided gate oxide layer away from the semiconductor substrate.

Yasushi teaches for each substrate in a batch of semiconductor substrates, nitriding a gate oxide layer on the semiconductor substrate to form the nitrided gate oxide layer on the substrate, oxidizing the nitrided gate oxide layer on the substrate to form an oxidized nitrided gate oxide layer, wherein the step of oxidizing the nitrided gate oxide layer distances the nitrided gate oxide layer away from the semiconductor substrate (Yasushi does not expressly teach this effect, but since Yasushi teaches reoxidizing the nitrided gate manner by heating the sample in an oxygen atmosphere—page 2, lines 6-8 of the translation—the same method disclosed by Applicant, it is inherent that the step of oxidizing the nitrided gate oxide layer taught by Yasushi will also distance the nitrided gate oxide layer away from the semiconductor substrate), and measuring the thickness of the oxidized nitrided gate oxide layer with a film thickness measuring device. Yasushi also teaches correlating the thickness of the reoxidized nitrided gate oxide layer with nitrogen concentration.

Yasushi does not teach using nitric oxide (NO) gas to form the nitrided gate oxide layer.

Bensa hel et al. teaches that it is known in the art to substitute NO for $N_2O$ to nitride a gate oxide layer because $N_20$ is ineffective for nitriding thin oxide layers (column 1, lines 35-40).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Yasushi and substitute NO for $N_2O$ to nitride the gate oxide layer because it is known in the art to use either NO or $N_2O$ for this purpose, and furthermore, $N_2O$ is ineffective for nitriding thin oxide layers, as expressly taught by Bensahel et al.

It would also have been obvious to one of ordinary skill in the art, at the time of the invention, to combine the teaching of Li with the combined teachings of Yasushi and Bensahel et al. by incorporating with the teachings of Li the steps of, for each substrate in a batch of semiconductor substrates, nitriding a gate oxide layer on the semiconductor substrate using nitric oxide gas to form the nitrided gate oxide layer on the substrate, and oxidizing the nitrided gate oxide layer on the substrate to form an oxidized nitrided gate oxide layer, and measuring the thickness of the oxidized nitrided gate oxide layer, in order to determine the nitrogen concentration in the gate oxide layer.

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li (U.S. 5,862,054) in view of Yasushi (JP 2000-311928, published 11/7/2000) and Bensahel et

al. (U.S. 6,372,581), as applied to claim 19 above, and further in view of Wolf et al. (*Silicon Processing for the VLSI Era*, vol. 1-3).

Regarding claim 23, Li, Yasushi, and Bensahel et al. together teach the method of claim 19 (note 35 U.S.C. 103(a) rejection above). Yasushi further teaches forming a gate electrode over the gate oxide layer (abstract, pg. 2—although Yasushi does not explicitly teach forming the gate electrode layer, the Examiner deems this step inherent to the disclosure of Yasushi, since the scope of Yasushi's teaching entails a method for measuring the nitrogen concentration specifically in a gate oxide film (see MPEP 2112). They do not teach implanting boron atoms in the gate electrode layer.

However, Wolf et al. teaches that it is known in the art to implant boron into a polysilicon gate electrode to make a p+ gate electrode, particularly with thin-oxide devices, to decrease punchthrough problems (vol. 3, pgs. 311-312).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Li, Yasushi and Bensahel et al. together, and also taught by claim 19, and further form a gate electrode layer, taught by Yasushi, and implant boron into the gate electrode to decrease punchthrough problems, as expressly taught by Wolf et al.

***Response to Arguments***

Applicant's arguments filed 1/31/2006 have been fully considered but they are not persuasive.

Regarding all of the claims, Applicant's primary argument is that the combination of Yasushi and Bensahel does not teach that the step of oxidizing the nitrided gate

oxide layer distances the nitrided gate oxide layer away from the semiconductor substrate, a limitation added by amendment. Applicant additionally argues that Bensahel teaches away from this step, since the prior-art method described by Bensahel "does not allow the presence of nitrogen to be localized precisely at the interface between the substrate and the gate oxide layer ($Si/SiO_2$) interface" (p. 7, fourth paragraph).

However, these arguments are not persuasive because Applicant does not claim or disclose which feature of the reoxidation process results in the nitrided gate oxide layer being distanced away from the semiconductor substrate. As best understood by the Examiner, the reoxidation process taught by Applicant comprises heating the nitrided gate oxide in an oxygen atmosphere (last paragraph of page 9 in the instant specification), which is the same as the reoxidation process taught by Yasushi. There is therefore no indication that Applicant's reoxidation process would produce results different from Yasushi's.

Additionally, the rejections presented in this and the last Office action rely upon the teachings of Bensahel only to establish the obviousness of using NO instead of $N_2O$ to nitride an oxide layer (Applicant additionally discloses that in the instant invention either NO or $N_2O$ can be used in the nitridation step—see second full paragraph on p. 9). The disclosure of Yasushi is relied upon to teach the reoxidation step, and as discussed above, Applicant does not disclose or claim the criticality of any particular reoxidation step or process in producing a distance between the nitrided gate oxide layer and the substrate. Absent some such teaching, it is inherent that the reoxidation

process taught by Yasushi will have the same result as the reoxidation process taught by Applicant, since they both comprise heating the substrate in an oxygen atmosphere.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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